EXHIBIT 1

Joint Claim Construction Chart

1. U.S. Patent No. 7,619,912

	Term, Phrase, or Clause	Netlist's Proposed Construction	Samsung's Proposed Construction	Micron's Proposed Construction	Court's Construction
1.	"rank" (All claims)	A "rank" of "DDR memory devices" is "a predetermined group of DDR memory devices on a memory module that can send or receive a fixed number of data bits via a fixed width data bus, in response to a read or write command and independently from other DDR memory devices on the memory module."	"an independent set of one or more memory devices on a memory module that act together in response to command signals, including chip-select signals, to read or write the full bit-width of the memory module"	"an independent set of one or more memory devices on a memory module that act together in response to command signals, including chip select signals, to read or write the full bit-width of the memory module"	
2.	"A memory module connectable to a computer system, the memory module comprising" (All claims)	Preamble is limiting; and plain and ordinary meaning	Preamble not limiting. Plain and ordinary meaning	Preamble not limiting. Plain and ordinary meaning	
3.	"signal" (All claims)	Plain and ordinary meaning	"a varying electrical impulse that conveys information from one point to another"	"a varying electrical impulse that conveys information from one point to another"	

	Term, Phrase, or Clause	Netlist's Proposed Construction	Samsung's Proposed Construction	Micron's Proposed Construction	Court's Construction
4.	"row[/column] address signal" (All claims)	Plain and ordinary meaning	"a varying electrical impulse that conveys an address of either a row or a column of memory locations from one point to another"	"a varying electrical impulse that conveys an address of either a row or a column of memory locations from one point to another"	
5.	"wherein the logic element generates gated column access strobe (CAS) signals or chip-select signals of the output [control] signals in response at least in part to (i) the [at least one] row address signal, (ii) the bank address signals, and (iii) the [at least one] chip-select signal of the [set/plurality] of input [control] signals and (iv) the PLL clock signal" (Claims 1, 15, 28, 39)	Plain and ordinary meaning	"the logic element generates gated column access strobe signals or chip-select signals in response at least in part to all four of (i) the at least one row address signal, (ii) the bank address signals, (iii) the at least one chip-select signal of the set of input control signals and (iv) the PLL clock signal"	"the logic element generates gated column access strobe signals or chip-select signals in response at least in part to all four of (i) the at least one row address signal, (ii) the bank address signals, (iii) the at least one chip-select signal of the set of input control signals and (iv) the PLL clock signal"	
6.	"wherein the logic element responds to at least (i) a row address bit of the at least one	Plain and ordinary meaning	"the logic element generates a number of chip-select signals equal to the first number of	"the logic element generates a number of chip-select signals equal to the first number of	

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	row/column address signal, (ii) the bank signals, and (iii) the at least one chip-select signal of the set of input control signals and (iv) the PLL clock by generating a first number of chip-select signals of the set of output control signals, the first number of chip-select signals generated by the logic element equal to the first number of ranks, and the at least one chip-select signal of the set of input control signals comprises a second number of chip-select signals equal to the second number of ranks" (Claim 77)		ranks in response to all four of (i) a row address bit of the at least one row/column address signal, (ii) the bank address signals, (iii) a number of chip-select signals of the set of input control signals equal to the second number of ranks and (iv) the PLL clock signal"	ranks in response to all four of (i) a row address bit of the at least one row/column address signal, (ii) the bank address signals, (iii) a number of chip-select signals of the set of input control signals equal to the second number of ranks and (iv) the PLL clock signal"	

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7.	"wherein the generation of the first number of chip-select signals of the output control signals by the logic element is based on the logic element responsive at least in part to (i) the at least one row address signal, (ii) the bank address signals, and (iii) the at least one chip-select signal of the set of input control signals received by the logic element and (iv) the clock signals received from the phase-lock loop device" (Claim 80)	Plain and ordinary meaning	"the logic element generates the first number of chip-select signals in response at least in part to all four of (i) the at least one row address signal, (ii) the bank address signals, (iii) the at least one chip-select signal of the set of input control signals and (iv) the PLL clock signal"	"the logic element generates the first number of chip-select signals in response at least in part to all four of (i) the at least one row address signal, (ii) the bank address signals, (iii) the at least one chip-select signal of the set of input control signals and (iv) the PLL clock signal"	
8.	"wherein the logic element responds to at least the at least one row address signal, the bank address signals, and the at least one chip-select signal of	Plain and ordinary meaning	"the logic element generates a number of rank-selecting signals greater than or equal to double the number of input chip-select signals in response to all four of	"the logic element generates a number of rank-selecting signals greater than or equal to double the number of input chip-select signals in response to all four of	

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	the set of input [control] signals and the PLL clock signal by generating a number of rank-selecting signals of the set of output [control] signals that is greater than double or equal to double the number of chip-select signals of the set of input [control] signals" (Claim 82, 86)		(i) the at least one row address signal, (ii) the bank address signals, (iii) the at least one chip-select signal of the set of input control signals and (iv) the PLL clock signal"	(i) the at least one row address signal, (ii) the bank address signals, (iii) the at least one chip-select signal of the set of input control signals and (iv) the PLL clock signal"	
9.	"wherein the logic element responds to at least (i) the row address signal, (ii) the bank address signals, (iii) and the one chip-select signal of the set of input control signals and (iv) the PLL clock signal by generating a number of rank-selecting signals of the set of output signals that is greater than double or	Plain and ordinary meaning	"the logic element generates a number of rank-selecting signals greater than or equal to double the number of input chip-select signals in response to all four of (i) the at least one row address signal, (ii) the bank address signals, (iii) the at least one chip-select signal of the set of input control signals and (iv) the PLL clock signal"	"the logic element generates a number of rank-selecting signals greater than or equal to double the number of input chip-select signals in response to all four of (i) the at least one row address signal, (ii) the bank address signals, (iii) the at least one chip-select signal of the set of input control signals and (iv) the PLL clock signal"	

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	equal to double the number of chip-select signals of the set of input control signals" (Claim 88)				
10.	"wherein the logic element responds to at least (i) the at least one row signal, (ii) the bank address signals, (iii) and the second number of chip-select signals of the plurality of input signals and (iv) the PLL clock signal by generating the first number of chip-select signals of the plurality of output signals that is greater than double or equal to double the second number of chip-select signals of the plurality of input signals" (Claim 90)	Plain and ordinary meaning	"the logic element generates a number of chip select signals greater than or equal to double the number of input chip-select signals in response to all of (i) the at least one row address signal, (ii) the bank address signals, (iii) the second number of chip-select signals of the set of input control signals and (iv) the PLL clock signal"	"the logic element generates a number of chip select signals greater than or equal to double the number of input chip-select signals in response to all of (i) the at least one row address signal, (ii) the bank address signals, (iii) the second number of chip-select signals of the set of input control signals and (iv) the PLL clock signal"	

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11.	"coupled to the printed circuit board" (Claims 15, 16, 28, 86, 88)	[AGREED]	[AGREED]	[AGREED]	"electrically connected to the printed circuit board"
12.	"mounted to the printed circuit board" (Claims 1, 39, 77, 80, 82, 90)	[AGREED]	[AGREED]	[AGREED]	"attached to the printed circuit board"

2. U.S. Patent No. 9,858,215

	Term, Phrase, or Clause	Netlist's Proposed Construction	Samsung's Proposed Construction	Micron's Proposed Construction	Court's Construction
13.	"A memory module operable in a computer system to communicate data with a memory controller of the computer system via a memory bus in response to memory commands received from the memory controller, the memory commands including a first memory command and a subsequent second memory command, the first memory command to cause the memory module to receive or output a first data burst and the second memory command to cause the memory module to receive or output a second data burst, the memory module comprising:"; (Claim 1)	[AGREED]	[AGREED]	[AGREED]	The preamble is limiting.
14.	"rank" (All claims)	"a predetermined group of memory integrated circuits on a memory module that can send or receive a fixed number of data bits via a fixed width data bus, in response	"an independent set of one or more memory devices on a memory module that act together in response to command signals, including chip-select	"an independent set of one or more memory devices on a memory module that act together in response to command signals, including chip-select signals, to read or	

	Term, Phrase, or Clause	Netlist's Proposed Construction	Samsung's Proposed Construction	Micron's Proposed Construction	Court's Construction
		to a read or write command and independently from other memory integrated circuits on the memory module"	signals, to read or write the full bit-width of the memory module"	write the full bit-width of the memory module"	
15.	"operable in a computer system to communicate data" (Claim 1)	Plain and ordinary meaning	"configured in a computer system to communicate data"	"configured in a computer system to communicate data"	
16.	"logic coupled to the buffer and configured to respond to the first memory command by providing first control signals to the buffer to enable communication of the first data burst between the at least one first memory integrated circuit and the memory controller through the buffer"; (Claim 1)	Plain and ordinary meaning, that is, the limitation does not require the first rank and second rank of memory integrated circuits to be on different forks and the term is not a 112(b) term.	"logic coupled to the buffer and configured to respond to the first memory command by providing first control signals to selectively electrically couple the input of the buffer to a first data signal line at the output of the data buffer to enable communication of the first data burst between the at least one first memory	The identified "logic" features (*see also* term 17) in claim 1 are indefinite. For claim 1, the "logic" features are subject to §112, ¶ 6, but there is no disclosure of adequate structure or algorithm for the functions of: (i) respond[ing] to the first memory command by providing first control signals to the buffer to enable communication of the first data burst between the at least one	

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			integrated circuit and the memory controller through the buffer, and disabling a second data signal line at the output of the buffer connected to the second memory integrated circuit"	first memory integrated circuit and the memory controller through the buffer; and (ii) further respond[ing] to the second memory command by providing second control signals to the buffer to enable communication of the second data burst between the at least one second memory integrated circuit and the memory controller through the buffer.	
17.	"wherein the logic is further configured to respond to the second memory command by providing second control signals to the buffer to enable communication of the second data burst between the at least one second memory integrated circuit and the memory controller through the buffer, the second control signals being different from the first control signals"	Plain and ordinary meaning, that is, the limitation does not require the first rank and second rank of memory integrated circuits to be on different forks and the term is not a 112(b) term.	"wherein logic is further configured to respond to the second memory command by providing second control signals to selectively electrically couple the input of the buffer to a second data signal line at the output of the	*See* proposed construction for term 16.	

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	(Claim 1)		data buffer to enable communication of the second data burst between the at least one second memory integrated circuit and the memory controller through the buffer, and disabling a first data signal line at the output of the buffer connected to the first memory integrated circuit"		
18.	"A method of operating a memory module coupled to a memory controller via a memory bus, the memory module comprising memory integrated circuits arranged in ranks and mounted on a printed circuit board having a plurality of edge connections coupled to the memory bus, the memory integrated circuits including at least one first memory integrated circuit in a first rank and at least one second memory integrated	[AGREED]	[AGREED]	[AGREED]	The preamble is limiting.

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	circuit in a second rank, the method comprising:" (Claim 21)				
19.	"in response to the first memory command, providing first control signal to a buffer to enable communication of the first data burst between the at least one first memory integrated circuit and the memory controller through the buffer"; and (Claim 21)	Plain and ordinary meaning, that is, the limitation does not require the first rank and second rank of memory integrated circuits to be on different forks and the term is not a 112(b) term.	"in response to the first memory command, providing first control signals to selectively electrically couple the input of the buffer to a first data signal line at the output of the data buffer to enable communication of the first data burst between the at least one first memory integrated circuit and the memory controller through the buffer, and disabling a second data signal line at the output of the buffer connected to	N/A	

	Term, Phrase, or Clause	Netlist's Proposed Construction	Samsung's Proposed Construction	Micron's Proposed Construction	Court's Construction
			the second memory integrated circuit"		
20.	"in response to the second memory command, providing second control signals to the buffer to enable communication of the second data burst between the at least one second memory integrated circuit and the memory controller through the buffer, the second control signals being different from the first control signals" (Claim 21)	Plain and ordinary meaning, that is, the limitation does not require the first rank and second rank of memory integrated circuits to be on different forks and the term is not a 112(b) term.	"in response to the second memory command, providing second control signals to selectively electrically couple the input of the buffer to a second data signal line at the output of the data buffer to enable communication of the second data burst between the at least one second memory integrated circuit and the memory controller through the buffer, and disabling a first data signal line at the output of the buffer connected to the first memory integrated circuit"	N/A	

	Term, Phrase, or Clause	Netlist's Proposed Construction	Samsung's Proposed Construction	Micron's Proposed Construction	Court's Construction
21.	"the memory module has an overall CAS latency" / "overall CAS latency of the memory module" (Claims 3, 4, 24, 25)	Plain and ordinary meaning	Plain and ordinary meaning.	"the delay between: (1) the time when a read command is executed by the memory module, and (2) the time when the first piece of data is made available at an output of the memory module"	
22.	"actual operational CAS latency of each of the plurality of memory integrated circuits" / "actual operational CAS latency of the memory integrated circuits" (Claims 3, 4, 24, 25)	Plain and ordinary meaning	Plain and ordinary meaning.	"the delay between: (1) the time when a read command is executed by each of the plurality of memory integrated circuits, and (2) the time when the first piece of data is made available at an output of each of the plurality of memory integrated circuits" / "the delay between: (1) the time when a read command is executed by the memory integrated circuits, and (2) the time when the first piece of data is made available at an output of the memory integrated circuits"	

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23.	"burst of data strobe signals" (Claims 12, 13, 28, 29)	Plain and ordinary meaning	Plain and ordinary meaning.	Indefinite.	
24.	"the at least one of the circuit components" (Claim 15)	Plain and ordinary meaning	Plain and ordinary meaning.	Indefinite.	

3. U.S. Patent No. 11,093,417

	Term, Phrase, or Clause	Netlist's Proposed Construction	Samsung's Proposed Construction	Micron's Proposed Construction	Court's Construction
25.	"A memory module operable in a computer system to communicate data with a memory controller of the computer system via a N-bit wide memory bus in response to read or write memory commands received from the memory controller, the memory bus including address and control signal lines and data signal lines, the memory module comprising:" (Claim 1)	[AGREED]	[AGREED]	[AGREED]	The preamble is limiting
26.	"rank" (All claims)	"a predetermined group of memory devices on a memory module that can send or receive a fixed number of data bits	"an independent set of one or more memory devices on a memory module that act together in response to command signals, including chip-	"an independent set of one or more memory devices on a memory module that act together in response to command signals, including chip-select	

	Term, Phrase, or Clause	Netlist's Proposed Construction	Samsung's Proposed Construction	Micron's Proposed Construction	Court's Construction
		via a fixed width data bus, in response to a read or write command and independently from other memory devices on the memory module"	select signals, to read or write the full bit-width of the memory module"	signals, to read or write the full bit-width of the memory module"	
27.	"operable in a computer system to communicate data" (Claim 1)	Plain and ordinary meaning	"configured in a computer system to communicate data"	"configured in a computer system to communicate data"	
28.	"data buffer control signals" (Claims 1, 3, 11)	Plain and ordinary meaning	"a signal sent to a buffer to selectively electrically couple the data signal line at the input of the buffer to a first signal line and a second signal line at the output of the buffer wherein each of the first signal line and the second signal line is connected to a different rank"	*See* proposed constructions for terms 29, 31, and 32.	
29.	"circuitry coupled between the data signal lines in the N-	Plain and ordinary meaning, that is, the limitation does not	"a data buffer coupled between the data signal lines in the N-bit wide	The identified "circuitry" feature in claim 1 is indefinite.	

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	bit wide memory bus and corresponding data pins of memory devices in each of the plurality of N-bit wide ranks, the circuitry being configurable to transfer the burst of N-bit wide data signals between the N-bit wide memory bus and the memory devices in the one of the plurality of N-bit wide ranks in response to the data buffer control signal" (Claim 1)	require the first rank and second rank of memory integrated circuits to be on different forks and the term is not a 112(b) term.	memory bus and corresponding data pins of memory devices in each of the plurality of N-bit wide ranks, the buffer configurable to selectively electrically couple a single data signal line at the input of the buffer to a first signal line and second signal line at the output of the buffer to transfer N-bit wide data signals between the N-bit wide memory bus and the memory devices in the one of the plurality of N-bit wide rank, wherein each signal line at the output of the buffer is connected to a different N-bit wide rank."	For claim 1, the "circuitry" feature is subject to §112, ¶ 6, but there is no disclosure of adequate structure or algorithm for the function of: transfer[ring] the burst of N-bit wide data signals between the N-bit wide memory bus and the memory devices in the one of the plurality of N-bit wide ranks in response to the data buffer control signal.	
30.	"circuitry includes logic pipelines configurable to enable the data transfers between the memory devices and the	Plain and ordinary meaning	Plain and ordinary meaning.	The identified "circuitry" features in claims 6 and 11 (*see* term 31) are indefinite. For claims 6 and 11, the "circuitry" features are	

	Term, Phrase, or Clause	Netlist's Proposed Construction	Samsung's Proposed Construction	Micron's Proposed Construction	Court's Construction
	memory bus through the circuitry" (Claim 6)			subject to §112, ¶ 6, but there is no disclosure of adequate structure or algorithm for the functions of: (i) the circuitry (of claim 1) includ[ing] logic pipelines configur[ed] to enable the data transfers between the memory devices and the memory bus through the circuitry; and (ii) enabl[ing] the data paths in response to the data buffer control signals so that the burst of N-bit wide data signals are transferred via the data paths.	
31.	"circuitry is configurable to enable the data paths in response to the data buffer control signals so that the burst of N-bit wide data signals are transferred via the data paths"	Plain and ordinary meaning, not a 112(6) term	Plain and ordinary meaning.	*See* proposed construction for term 30.	

	Term, Phrase, or Clause	Netlist's Proposed Construction	Samsung's Proposed Construction	Micron's Proposed Construction	Court's Construction
	(Claim 11)				
32.	"logic . . . configurable to receive a set of input address and control signals associated with a read or write memory command via the address and control signal lines and to output a set of registered address and control signals in response to the set of input address and control signals, . . . the logic is further configurable to output data buffer control signals in response to the read or write memory command" (Claim 1)	Plain and ordinary meaning, not a 112(6) term	Plain and ordinary meaning.	The identified "logic" feature in claim 1 is indefinite. For claim 1, the "logic" feature is subject to §112, ¶ 6, but there is no disclosure of adequate structure or algorithm for the function of: output[ting] data buffer control signals in response to the read or write memory command.	
33.	"overall CAS latency of the memory module" (Claim 1)	Plain and ordinary meaning	Plain and ordinary meaning.	"the delay between: (1) the time when a read command is executed by the memory module, and (2) the time when the first	

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				piece of data is made available at an output of the memory module"	
34.	"actual operational CAS latency of each of the memory devices" (Claim 1)	Plain and ordinary meaning	Plain and ordinary meaning.	"the delay between: (1) the time when a read command is executed by each of the memory devices, and (2) the time when the first piece of data is made available at an output of each of the memory devices"	
35.	"wherein data transfers through the circuitry are registered for an amount of time delay such that the overall CAS latency of the memory module is greater than an actual operational CAS latency of each of the memory devices" (Claim 1)	Plain and ordinary meaning	Plain and ordinary meaning.	Indefinite.	

	Term, Phrase, or Clause	Netlist's Proposed Construction	Samsung's Proposed Construction	Micron's Proposed Construction	Court's Construction
36.	"the read or write command" (Claims 1, 15)	[AGREED]	[AGREED]	[AGREED]	"the read or write memory command"

4. U.S. Patent No. 10,268,608

	Term, Phrase, or Clause	Netlist's Proposed	Samsung's Proposed Construction	Court's Construction
37.	"A memory module operable to communicate with a memory controller via a memory bus, the memory bus including signal lines, the signal lines including a set of control/address signal lines and a plurality of sets of data/strobe signal lines, the memory module comprising" (Claim 1)	Preamble is limiting; and plain and ordinary meaning	Preamble not limiting. Plain and ordinary meaning	